LINEAR TECHNOLOGY DESIGN NOTES

High Efficiency I/O Power Generation for Mobile Pentium III Microprocessors – Design Note 258

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The demand for higher performance notebook computers has fueled the development of faster and more power-hogging microprocessors. These microprocessors also require a faster input/output (I/O) bus and a faster clock. From a power management perspective, this means that core, I/O and clock power supplies should be able to handle more power. This requires that core and I/O DC/DC converters operate more efficiently and be as small as possible. Linear Technology recommends the LTC®1778 to provide I/O power for the next generation Pentium® III microprocessors. The I/O input voltage requirement is 1.25V; transient (AC) tolerance is ±9% and static (DC) tolerance is ±5%. Load current requirements are as follows:

Processor V_{TT}: 2.7A

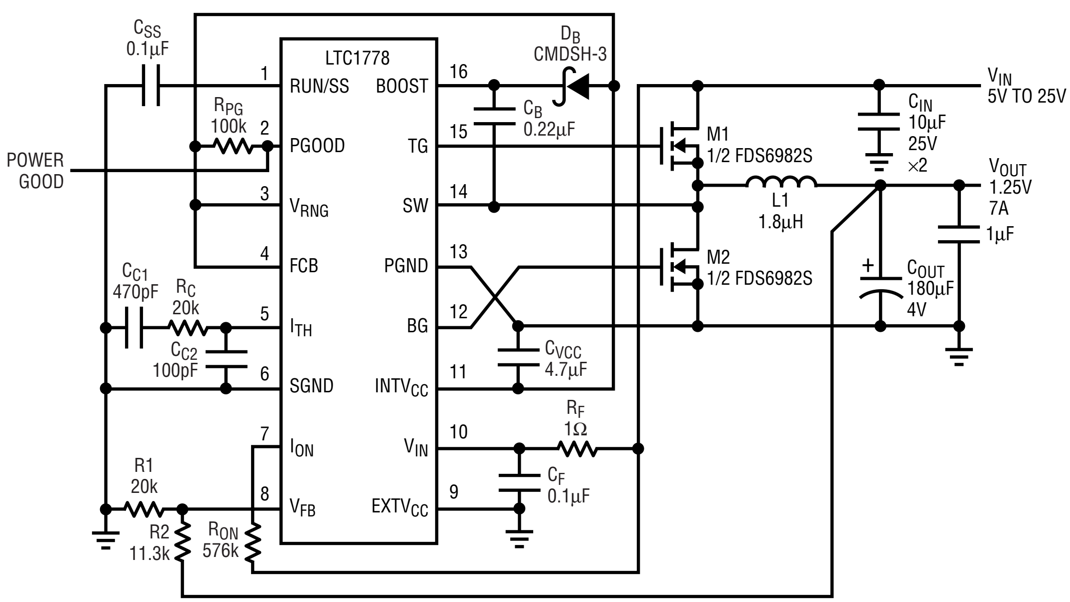
830M chipset V_{TT}: 0.7A

The 830M chipset core has the following two possibilities:

1. Internal graphics using the 830M engine: 3.6A
2. External AGP graphics: 1.6A

Total maximum I/O current: 7.0A

The LTC1778 is a synchronous step-down switching regulator controller that provides synchronous drive for two external N-channel MOSFET switches. The true current mode control architecture has an adjustable current limit, can be easily compensated, is stable with ceramic output capacitors and does not require a power-wasting sense resistor. An optional discontinuous mode of operation increases efficiency at light loads. The LTC1778 operates over a wide range of input voltages from 4V to



C_{IN}: TAIYO YUDEN TMK432BJ106MM
C_{OUT}: CORNELL DUBILIER ESRD181M02B
L1: TOKO 919AS-1R8N

Figure 1. LTC1778 Mobile Pentium III I/O Supply

36V and provides output voltages from 0.8 to 0.9 • V_{IN}. Switching frequencies up to nearly 2MHz can be chosen, allowing wide latitude in trading off efficiency for component size. Fault protection features include a power-good output, current limit foldback, optional short-circuit shutdown timer and an overvoltage soft latch. The LTC1778 is available in a 16-Lead narrow SSOP package.

Figure 1 shows a typical LTC1778 application schematic for a mobile Pentium III I/O supply. This circuit is optimized for small size and high efficiency from an input supply that varies from 5V to 24V. In order to reduce board space, it uses a single, dual N-channel FDS6982S MOSFET and only one 180µF (Panasonic SP) output capacitor. The superfast internal gate drivers with a typical rise time of 20ns help to minimize switching losses and the strong gate drivers help minimize conductive losses. Figure 2 shows the transient response for a 0A to 5.5A load step. It can be seen that the LTC1778 can easily meet the I/O transient and static specification with only one output capacitor. The LTC1778 allows the use of many different kinds of output capacitors such as aluminum electrolytic, tantalum, POSCAP, NEOCAP, SPs and ceramic, because of OPTI-LOOP™ compensation that allows the feedback loop to be compensated externally. Figure 3 shows the same output voltage transient with two 150µF POSCAP output capacitors. Note that the equivalent series resistance (ESR) of a POSCAP is 40mΩ, which is approximately twice that of an SP capacitor. Therefore, two POSCAPs are required to achieve the same output voltage transient response as one SP capacitor. Figure 4 shows typical efficiency curves for V_{IN} = 5V and V_{IN} = 15V, V_{OUT} = 1.25V, I_{LOAD} = 10mA to 7A. It can be seen that the efficiency is better than 85% for load currents up to 5A. The measured MOSFET case temperature is only 70°C for V_{IN} = 12V at I_{LOAD} = 7A. This circuit can be implemented on a 0.5" × 1" board space.

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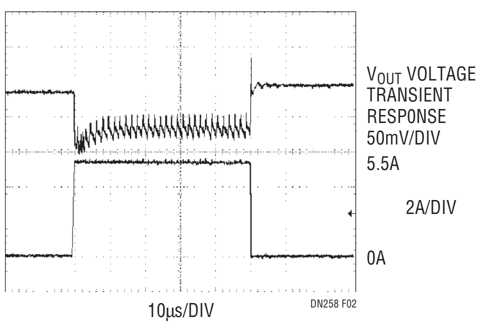

Figure 2. Output Voltage Transient Response for I_L = 0A to 5.5A with One SP Output Capacitor

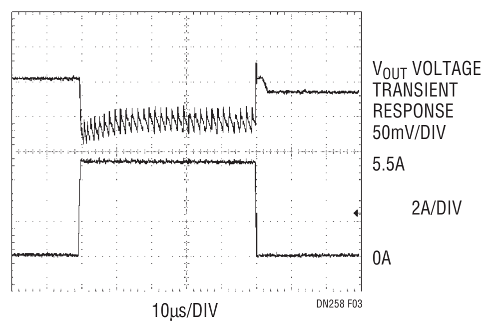

Figure 3. Output Voltage Transient Response for I_L = 0A to 5.5A with Two POSCAP Output Capacitors

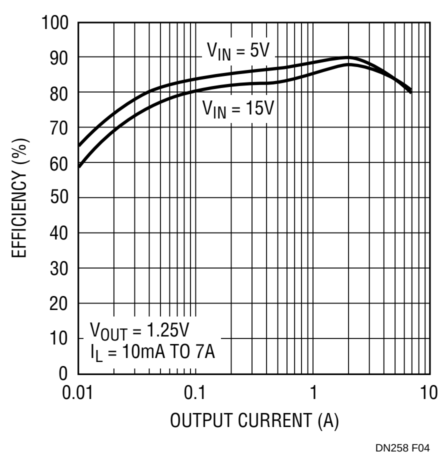

Figure 4. Efficiency Curves for Figure 1

Data Sheet Download

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